WHAT IS CLAIMED IS:

1. An apparatus for storing predicted return addresses of instructions being executed by a pipelined processor, the apparatus comprising:

a two part return address buffer, comprising

a speculative return address buffer; and

a committed return address buffer, both of which having multiple entries that may include predicted return addresses that have been pushed onto the return buffer.

2. The apparatus of claim 1 wherein when a predicted return address stored in the two part return buffer is popped, the predicted return address may come from either the speculative return address buffer or the committed address buffer.

3. The apparatus of claim 1 wherein the return address buffer stores return predicted RETURN addresses to allow recovery of predicted RETURN addresses in the case of mis-predicted instruction fetching.

4. The apparatus of claim 2 further comprising:

a read pointer pointing to a first entry in the speculative buffer;

a write pointer pointing to a second entry in the speculative buffer;

a processor that executes instructions to:

store a first return address in an entry in the speculative buffer, the entry being pointed to by the write pointer; and

read the first return address from the entry in the first set of entries, the entry being pointed to by the read pointer.

5. The apparatus of claim 4, wherein when a return address is stored in an entry of the speculative buffer the processor executes instructions to:

store the read pointer as a back pointer in the same entry,

set the read pointer equal to the value of the write pointer, and

increment the write pointer after the read pointer is set equal to the write pointer.

6. The apparatus of claim 2, wherein a number of entries included in the speculative buffer is specified, wherein when

the write pointer is incremented above the specified number the write pointer is set to point to the first entry in the speculative buffer.

7. The apparatus of claim 6, further comprising:

a storage device holding an SCOLOR indicator bit that is inverted each time the read pointer is set to point to the first or last entry in the speculative buffer; and

a bit storage location associated with each entry in the speculative buffer to hold the current value of SCOLOR each time a return address is written into the speculative buffer.

8. The apparatus of claim 4, further comprises:

retirement logic connected to the apparatus that indicates instructions that have completed execution in the processor, wherein when the retirement logic indicates an instruction has completed execution the return address corresponding to the completed instruction is written from the speculative buffer to the committed buffer.

9. The apparatus of claim 4, further comprising:

a storage location holding a pointer indicator bit to indicate the use of the speculative buffer or the committed buffer for reading a return address.

10. The apparatus of claim 9, wherein when the pointer indicator bit indicates the speculative buffer is to be used for reading the return address, the return address is read from the speculative buffer and the read pointer is set equal to the back address from the entry being read.

11. The apparatus of claim 10, further comprising:

a retirement logic block connected to the apparatus that indicates instructions that have completed execution in the processor,

wherein when the retirement logic indicates a CALL instruction has completed execution, the return address corresponding to the completed instruction is written from the speculative buffer to the committed buffer.

12. An article comprising a machine-readable medium that stores machine-executable instructions for storing predicted return addresses of instructions being executed by a pipelined processor, the instructions causing a machine to:

push a return address onto a two part return address buffer, wherein the two part buffer comprises a speculative return address buffer and a committed return address buffer, both of which having multiple entries; and

pop the predicted return address from the two part buffer, wherein the popped return address may come from either the speculative return address buffer or the committed address buffer.

13. The article of claim 12, further comprising instructions causing a machine to:

pop a return address from the committed buffer to allow recovery of predicted RETURN addresses in the case of mis-predicted instruction fetching.

14. The article of claim 13, further comprising instruction causing a machine to:

store a first return address in an entry in the speculative buffer, the entry being pointed to by the write pointer; and

read the first return address from the entry in the first set of entries, the entry being pointed to by the read pointer.

15. The article of claim 13, wherein pushing a return address onto the speculative buffer comprises instructions causing a machine to:

store the read pointer as a back pointer in the same entry;

set the read pointer equal to the value of the write pointer; and

increment the write pointer after the read pointer is set equal to the write pointer.

16. The article of claim 13, wherein a number of entries included in the speculative buffer is specified, wherein when the write pointer is incremented above the specified number the write pointer is set to point to the first entry in the speculative buffer.

17. The article of claim 16, wherein the instructions cause a machine to:

invert a storage device holding an SCOLOR indicator bit each time the read pointer is set to point to the first or last entry in the speculative buffer; and

store the SCOLOR indicator bit in an associated bit location each time a return address is written into the speculative buffer.

18. The article of claim 14, wherein retirement logic indicates an instruction has completed execution in the

processor, the return address corresponding to the completed instruction is written from the speculative buffer to the committed buffer.

19. The article of claim 14, wherein when a pointer indicator bit indicates the speculative buffer is to be used for reading the return address, the instructions cause a machine to:

read the return address from the speculative buffer; and

set the read pointer equal to the back address from the entry being read.

20. A method of storing predicted return addresses of instructions being executed by a pipelined processor, the method comprising:

pushing a return address onto a two part return address buffer, wherein the two part buffer comprises a speculative return address buffer and a committed return address buffer, both of which having multiple entries; and

popping the predicted return address from the two part buffer, wherein the popped return address may come from either the speculative return address buffer or the committed address buffer.

21. The method of claim 20, further comprising:

popping a return address from the committed buffer to allow recovery of predicted RETURN addresses in the case of mis-predicted instruction fetching.

22. The method of claim 21, further comprising:

storing a first return address in an entry in the speculative buffer, the entry being pointed to by the write pointer; and

reading the first return address from the entry in the first set of entries, the entry being pointed to by the read pointer.

23. The method of claim 21, wherein pushing a return address onto the speculative buffer comprises:

storing the read pointer as a back pointer in the same entry;

setting the read pointer equal to the value of the write pointer; and

incrementing the write pointer after the read pointer is set equal to the write pointer.

24. The method of claim 21, wherein a number of entries included in the speculative buffer is specified, wherein when

the write pointer is incremented above the specified number the write pointer is set to point to the first entry in the speculative buffer.

25. The method of claim 24, further comprising:

inverting a an SCOLOR indicator bit each time the read pointer is set to point to the first or last entry in the speculative buffer; and

storing the SCOLOR indicator bit in an associated bit location each time a return address is written into the speculative buffer.

26. The method of claim 22, wherein an indication that an instruction corresponding to a return address stored in the two part buffer has completed execution, the method further comprises:

writing the return address corresponding to the completed instruction from the speculative buffer to the committed buffer.

27. The method of claim 22, wherein when a pointer indicator bit indicates the speculative buffer is to be used for reading the return address, the instructions cause a machine to:

reading the return address from the speculative buffer; and

setting the read pointer equal to the back address from the entry being read.